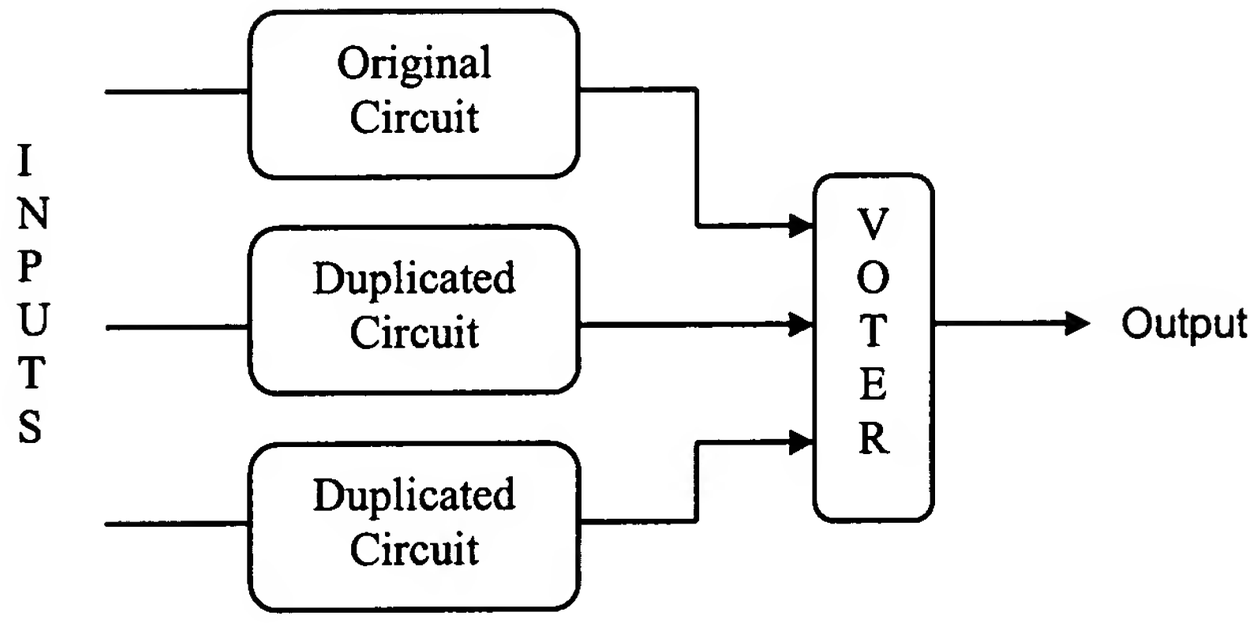
Fig. 1 Prior Art

1A



1B

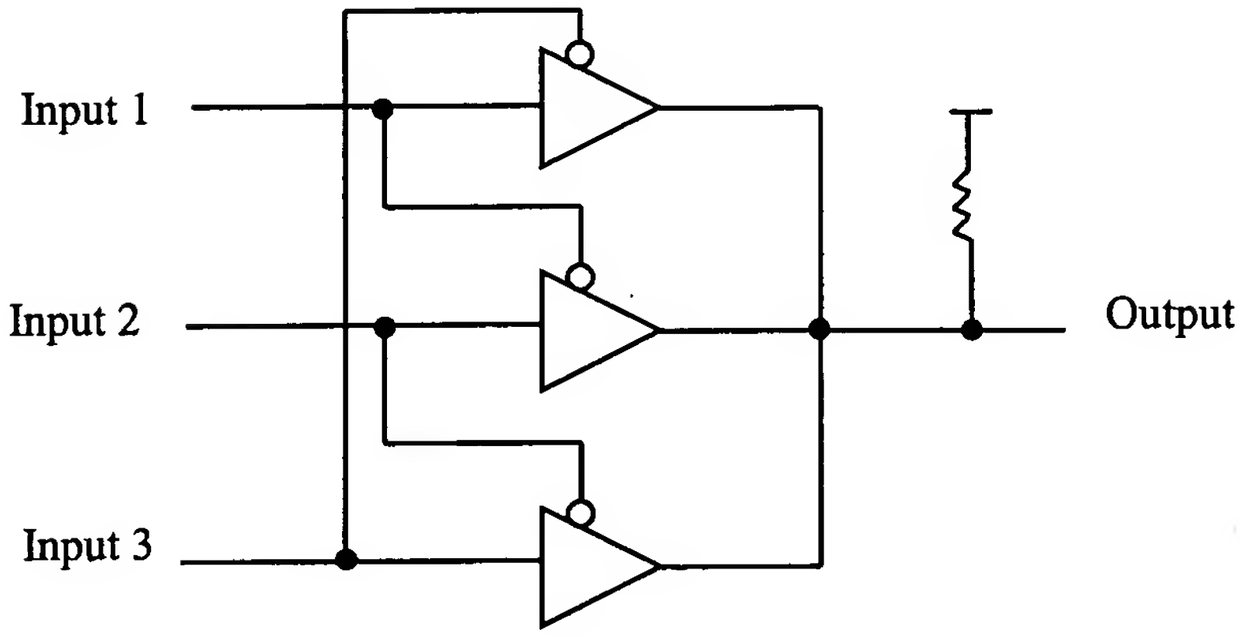
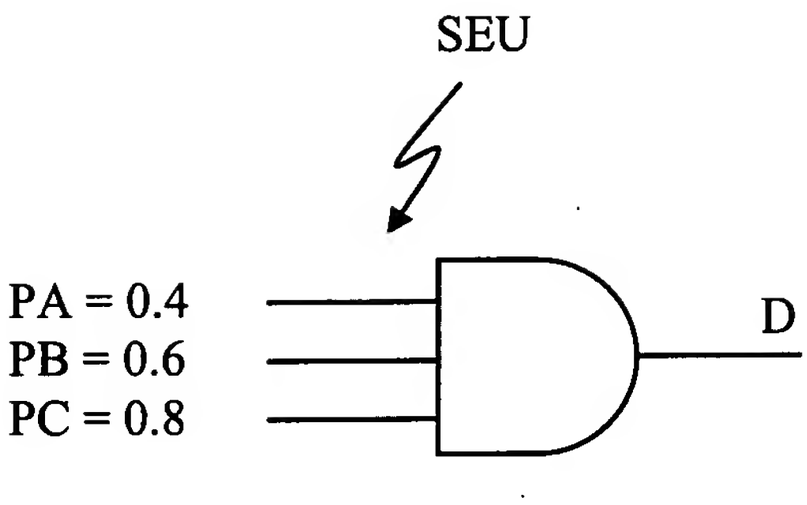


Fig. 2

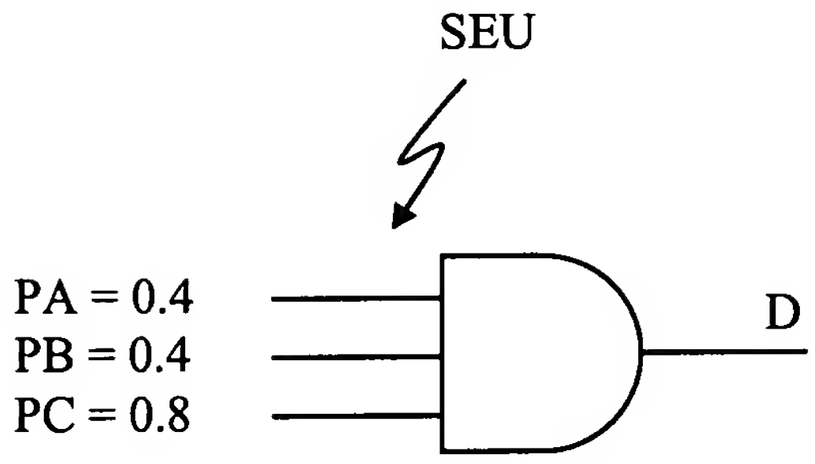
Gate Type	P_{out}
AND	$\Pi_i P_i$
NAND	$1-\Pi_i P_i$
OR	$\Sigma_i P_i - \Pi_i P_i$
NOR	$1-(\Sigma_i P_i - \Pi_i P_i)$
XOR	$\Sigma_{i,j} P(i)(1-P(j))$
XNOR	$1-(\Sigma_{i,j} P(i)(1-P(j)))$

Fig. 3



SEU-sensitive gate

Fig. 4



SEU-insensitive gate

Fig. 5

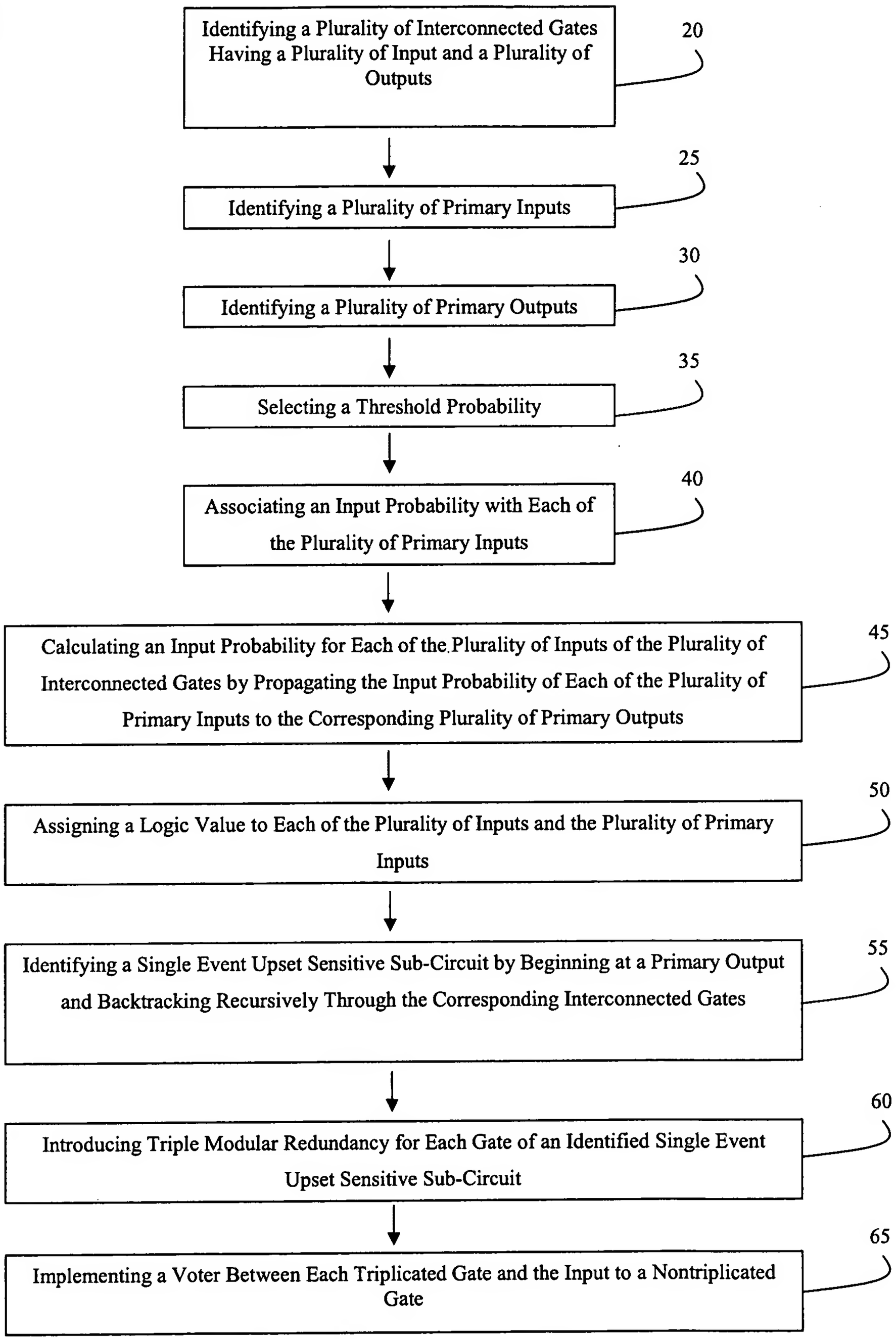
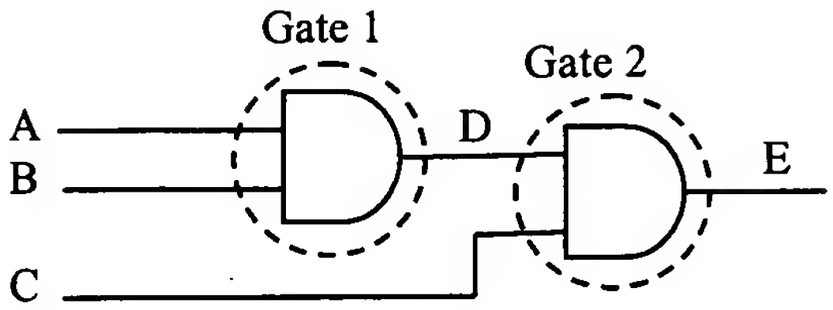
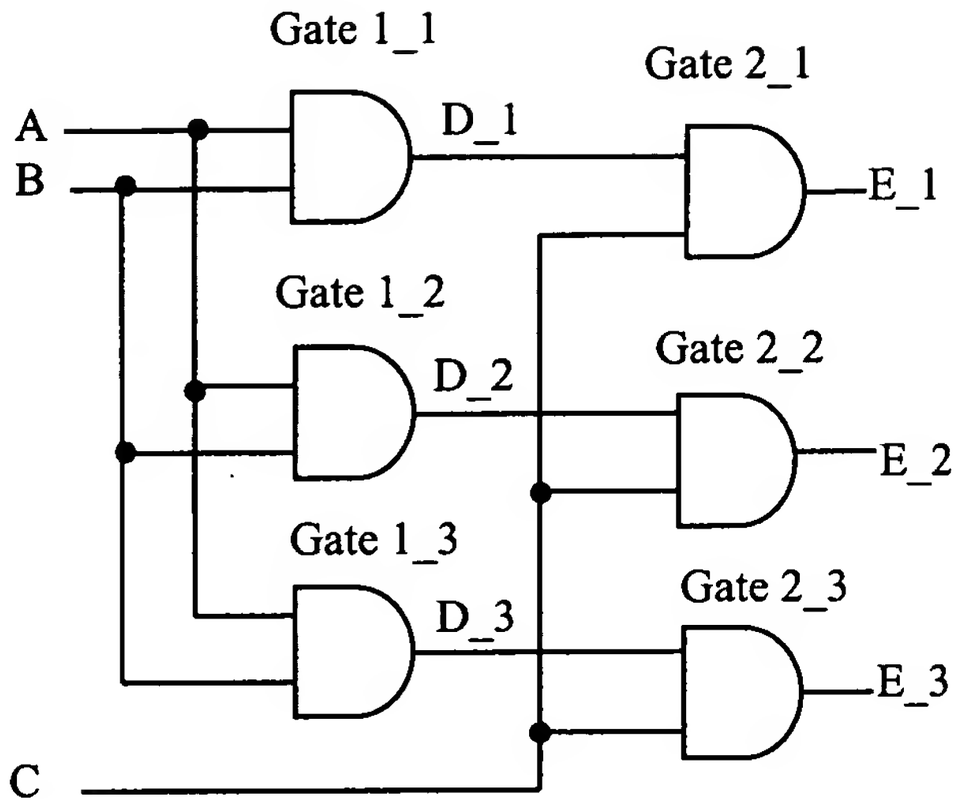

Identifying a Plurality of Interconnected Gates Having a Plurality of Input and a Plurality of Outputs
20
Identifying a Plurality of Primary Inputs
25
Identifying a Plurality of Primary Outputs
30
Selecting a Threshold Probability
35
Associating an Input Probability with Each of the Plurality of Primary Inputs
40
Calculating an Input Probability for Each of the Plurality of Inputs of the Plurality of Interconnected Gates by Propagating the Input Probability of Each of the Plurality of Primary Inputs to the Corresponding Plurality of Primary Outputs
45
Assigning a Logic Value to Each of the Plurality of Inputs and the Plurality of Primary Inputs
50
Identifying a Single Event Upset Sensitive Sub-Circuit by Beginning at a Primary Output and Backtracking Recursively Through the Corresponding Interconnected Gates
55
Introducing Triple Modular Redundancy for Each Gate of an Identified Single Event Upset Sensitive Sub-Circuit
60
Implementing a Voter Between Each Triplicated Gate and the Input to a Nontriplicated Gate
65

Fig. 6

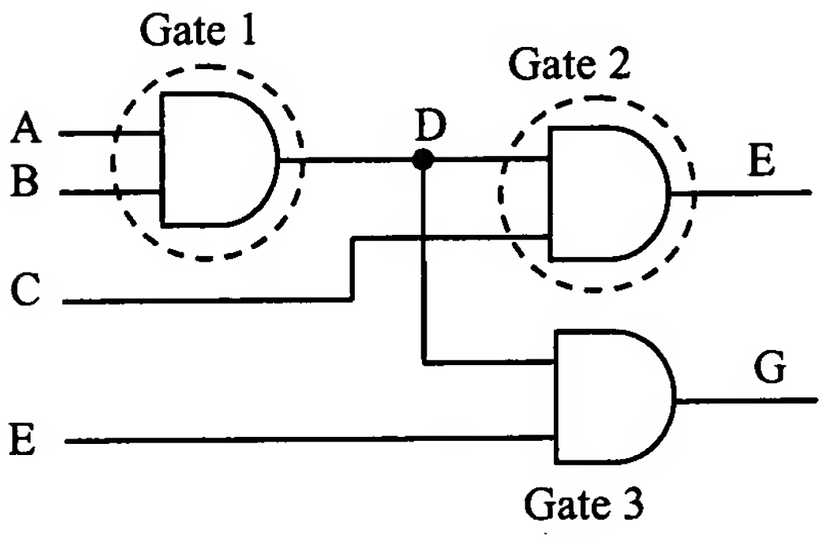
6A



6B



6C



6D

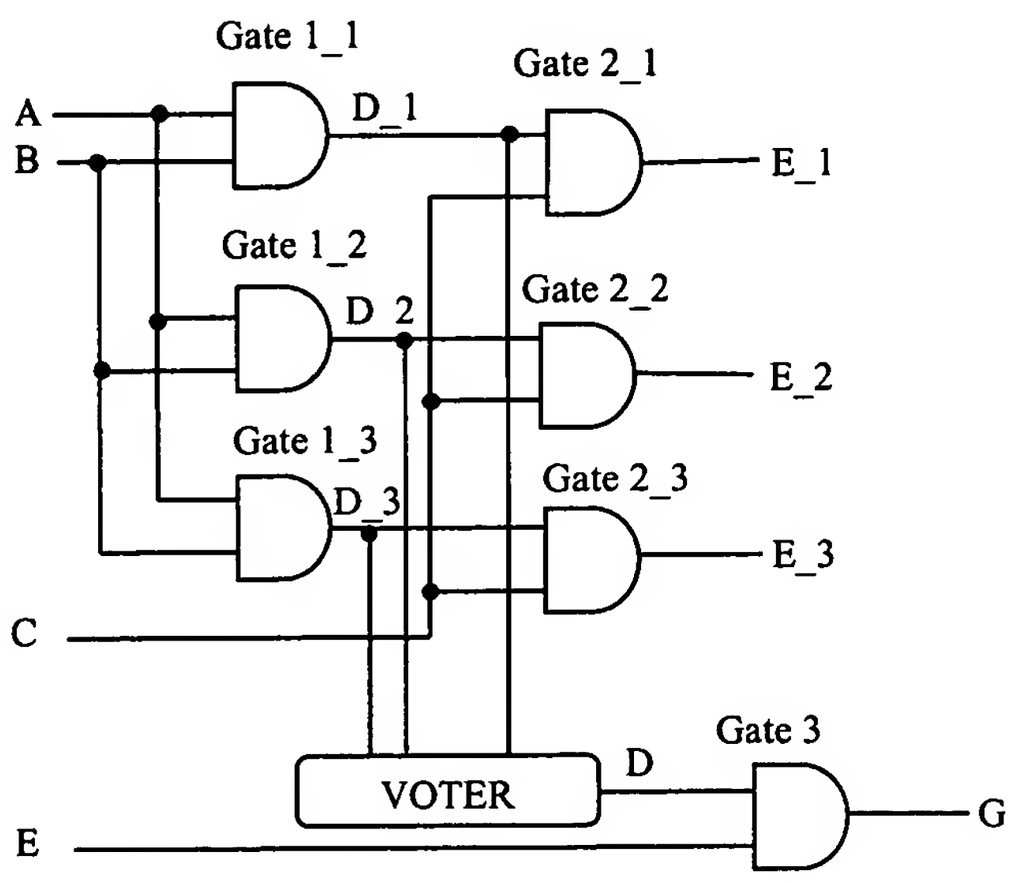


Fig. 7

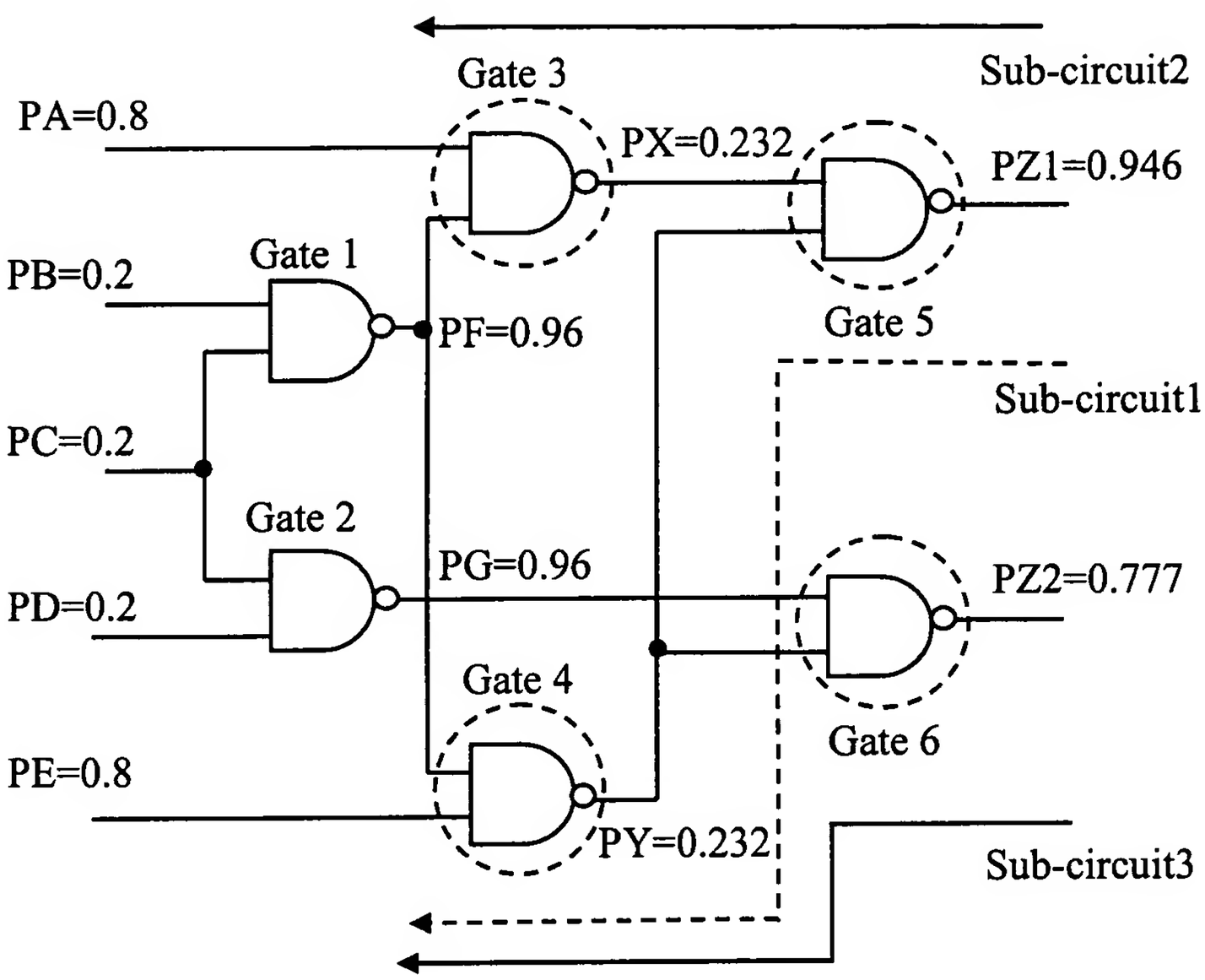
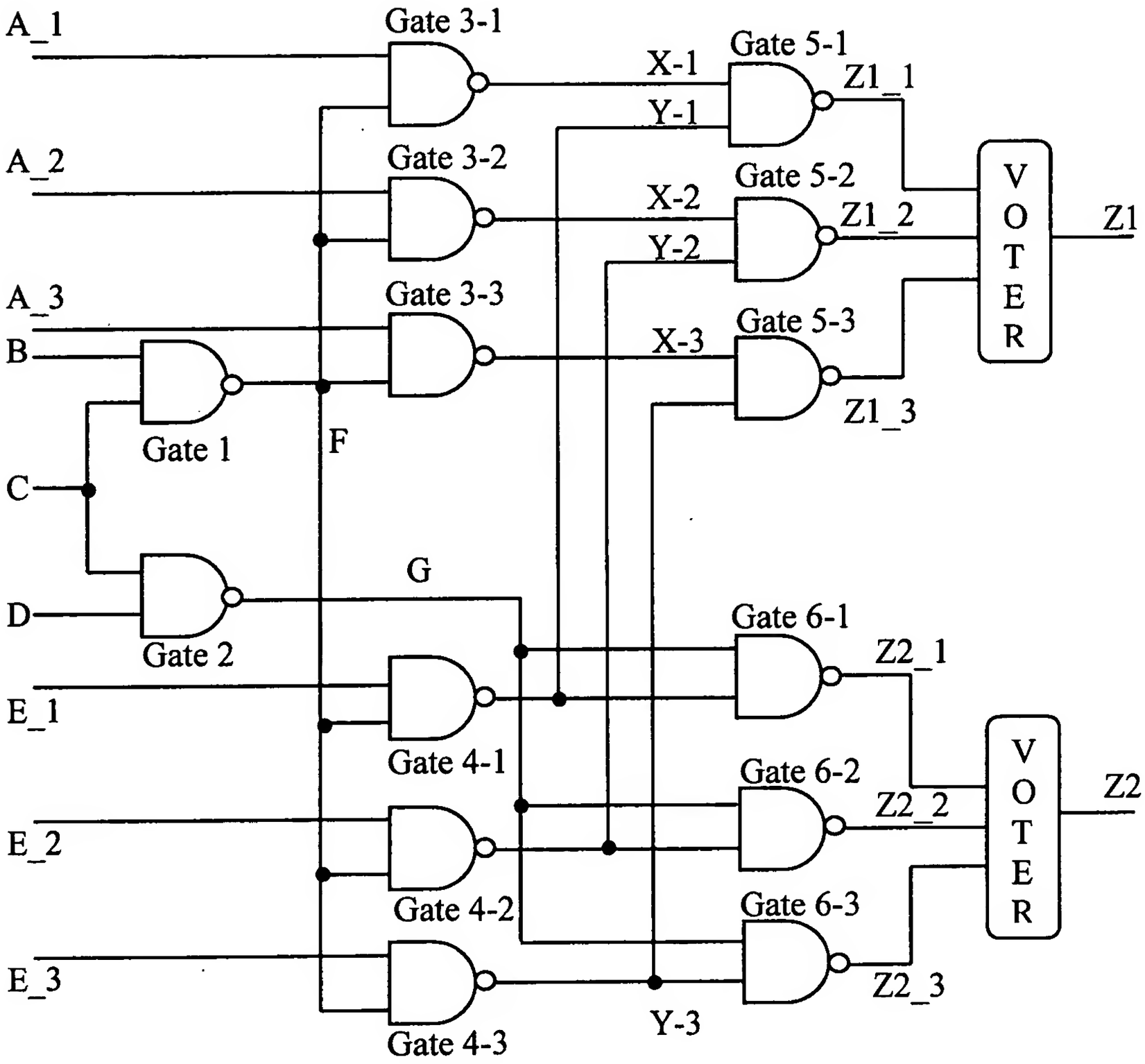

Gate 3
Sub-circuit2
PA=0.8
PX=0.232
PZ1=0.946
Gate 1
PB=0.2
PF=0.96
Gate 5
Sub-circuit1
PC=0.2
Gate 2
PG=0.96
PZ2=0.777
PD=0.2
Gate 4
Gate 6
PE=0.8
PY=0.232
Sub-circuit3

Fig. 8


A_1
Gate 3-1
X-1
Gate 5-1
Z1_1
Y-1
A_2
Gate 3-2
X-2
Gate 5-2
Z1_2
Y-2
V
O
T
E
R
Z1
A_3
Gate 3-3
X-3
Gate 5-3
Z1_3
B
Gate 1
F
C
G
D
Gate 2
Gate 6-1
Z2_1
E_1
Gate 4-1
Gate 6-2
Z2_2
Z2
E_2
Gate 4-2
Gate 6-3
Z2_3
E_3
Y-3
Gate 4-3